SF - 190

Total No. of Pages :3

Seat No.	

T.E. (Electronics Engineering) (Part - III) (Semester - VI) (Revised) Examination, November - 2017

VIDEO ENGINEERING

Sub. Code: 66852

Day and Date :Thursday, 02 - 11 - 2017 **Total Marks : 100**

Time :2.30 p.m. to 5.30 p.m.

Instructions : **1)** **All questions are compulsory.**

2) **Use suitable assumptions if required.**

3) **Draw necessary figures on right side of answer sheet.**

SECTION-I

Q1) Solve any three. **[18]**

a) Distinguish between positive and negative modulation.

b) What is horizontal and vertical resolution?

c) With suitable diagram describe how separation of U and V signals is achieved in colour TV.

d) Define the following terms related to T.V systems.

i) Aspect ratio

ii) hue

iii) brightness

iv) Saturation

e) Explain in brief the Mono & Stereophonic sound system in brief.

P.T.O.

Q2) Solve any two. **[16]**

a) Explain optical recording, & reproduction.

b) What is Scanning? Explain the need and the types of scanning with its merits and demerits.

c) Explain the typical composite video waveform and explain its various components.

Q3) Solve any two. **[16]**

a) What is compatibility and reverse compatibility? Explain how Colour sub carrier frequency is calculated to achieve frequency interleaving process.

b) Compare PAL and SECAM T.V. system.

c) Compare Delta-gun and Trinitron for its merit and Demerits.

SECTION-II

Q4) Answer any Three sub Questions. **[18]**

a) Explain Merits of Digital Technology.

b) Explain with a diagram, basic satellite system with uplink and down link Frequencies used for television.

c) With the help of suitable block diagram, Explain the different applications of CCTV.

d) Explain the general format of MAC signals for transmitting color Television Signals. What is the need of MAC encoding?

Q5) Attempt any Two Sub Questions. **[16]**

a) Draw and Explain Block schematic of the signal flow in video codec and the Video processor (ITT).

b) Draw and Explain the construction and working of LCD Television screen.

c) With Suitable Block Diagram explain the working of IR remote control used for Television receiver.

Q6) Attempt any Two sub Questions. **[16]**

a) Draw the Block diagram of Video codec VCU 2134 (ITT) and Explain digital signal processing carried out in it.

b) Draw the structure of Plasma Display Panel (PDP) used for television & Explain its working.

c) Draw and Explain Direct To Home Receiver system which can be employed for Distributing national television programs. What are the advantages & disadvantages of it.

SF-188

Total No. of Pages : 2

Seat No.	

T.E. (Electronics) (Part-III) (Semester-V) (Old) (Pre-Revised) Examination, November - 2017

CONTROL SYSTEM ENGINEERING

Sub. Code : 45593

Day and Date : Monday, 27-11-2017 **Total Marks : 100**

Time : 10.00 a.m. to 1.00 p.m.

Instructions : 1) **All questions are compulsory.**
2) **Assume suitable data if necessary.**

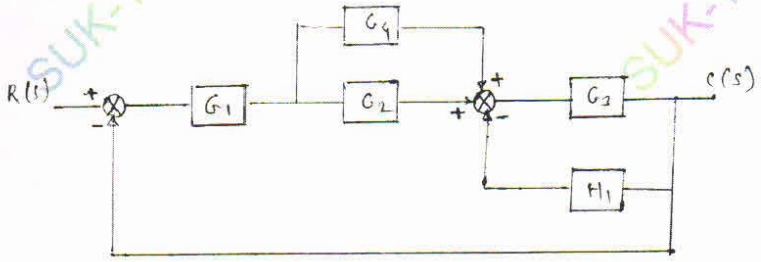
SECTION-I

Q1) Solve any two of the following. **[2×9=18]**

a) Explain mathematical modeling of Mechanical, Rotational & Electrical system.

b) Derive transfer Function of field controlled DC servo motor.

c) Reduce each block to a single block and determine transfer function.



Q2) Solve any two of the following. **[2×8=16]**

a) Derive steady state error for type zero, type one & type two system when step input is given.

b) The control system having unity feedback has

$$G(S) = \frac{20}{s(1+4s)(1+s)}$$

Determine k_p, k_v & k_a.

c) Classify open loop system & closed loop system with example.

P.T.O.

Q3) Solve any two of the following. **[2×8=16]**

a) Draw Root Locus for the system $G(s).H(S) = \frac{k}{s(s+3)(s+6)}$

b) Explain steps to solve Root Locus.

c) Explain in brief Reduction of parameter variations by use of feedback.

SECTION-II

Q4) Solve any two of the following. **[2×9=18]**

a) Explain steps to solve Bode Plot. Also explain Gain Margin & Phase Margin.

b) Solve Nyquist Plot $G(s).H(s) = \frac{1}{s(s+1)}$.

c) Find the Transfer function of the system

$$A = \begin{bmatrix} -2 & 1 & 0 \\ 0 & -3 & 1 \\ -3 & -4 & -5 \end{bmatrix} \quad B = \begin{matrix} 0 \\ 0 \\ 1 \end{matrix} \quad C = [0 \quad 1 \quad 0] \quad D = 0$$

Q5) Solve any two of the following. **[2×8=16]**

a) With the help of neat circuit diagram explain the PID Controller.

b) Solve Polar Plot

$$G(s).H(s) = \frac{500}{s(s+6)(s+9)}$$

c) Define State, state variable, state vector and state space.

Q6) Solve any two of the following. **[2×8=16]**

a) With the help of neat circuit diagram explain PLC controller.

b) Find controllability and observability.

$$A = \begin{bmatrix} -1 & 0 \\ 0 & -2 \end{bmatrix} \quad B = \begin{matrix} 0 \\ 1 \end{matrix} \quad C = [1 \quad 2]$$

c) With neat sketch Derive Lead compensator.

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SF - 182

Total No. of Pages :3

Seat No.	

T.E. (Electronics Engg.) (Part - III) (Semester - V) (Revised) Examination, November - 2017

MICROCONTROLLERS

Sub. Code: 66281

Day and Date :Saturday, 11 - 11 - 2017 **Total Marks : 100**
Time :10.00 a.m. to 1.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Assume suitable data if necessary.**
3) **Figures to the right indicate full marks.**

SECTION - I

Q1) Answer Any 4 of the following. **[5 marks each]**

a) Draw and explain internal RAM organization of 8051.

b) Compare between 89C51 RD2 and 89C420 Microcontrollers.

c) Draw a diagram indicating the external data memory interface to MCS-51.

d) Explain the JNB & JBC instructions of 8051 with suitable example.

e) Draw port - 3 internal structure and explain it briefly.

Q2) Answer Any Two of the following. **[8 marks each]**

a) Write ASM code to multiply the data bytes present at XRAM address 2000h & 2100h.

b) Draw H/W Interface of ADC 0809 to 8051 and explain it in brief.

c) Explain the Timer/Counter mode -3 of 8051 with suitable diagram.

P.T.O.

Q3) Answer Any Two of the following. **[7 marks each]**

a) What is meant by assembler directives? Explain the following.

i) ORG.

ii) EQU.

iii) END.

b) Draw a hardware interface of stepper motor to 8051 and explain it in brief.

c) Draw and explain interfacing of seven segment display to 8051.

SECTION - II

Q4) Answer Any TWO from the following. **[8 marks each]**

a) Write an Embedded - C program for 8051, to EXCHANGE block of five data bytes between external memory address (4000H) onwards & internal memory address (40H) onwards.

b) Draw and explain Program memory and Data memory organization in PIC 16F877.

c) Draw format and explain different bits of OPTION _ REG register.

Q5) Answer Any TWO from the following. **[8 marks each]**

a) Write a PIC 16F877 assembly language program to generate a square wave on port D pins using software delay.

b) Draw and explain loading of PC in different situations using PCL and PCLATH registers.

c) Explain ADC peripheral feature of PIC with respect to its channel selection and A/D result justification.

Q6) Answer any THREE from the following. **[6 marks each]**

a) Explain POR and BOR RESET options.

b) Explain different alternate multiplexed pin functions of PORTA of 16F877.

c) Describe Watchdog timer with block diagram.

d) Explain following instructions of 16F877.

i) MOVLW k

ii) SUBWF f, d

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SF - 184

Total No. of Pages :2

Seat No.	

T.E. (Electronics) (Semester - V) (Revised) Examination, November - 2017
VLSI DESIGN
Sub. Code: 66283

Day and Date :Monday, 20 - 11 - 2017 **Total Marks : 100**
Time :10.00 a.m. to 1.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to right indicate full marks.**
3) **Assume suitable data if necessary.**

SECTION-I

Q1) Attempt any THREE **[3×6=18]**

a) Write a VHDL description to implement "XOR gate" using 'when else' statement.

b) Explain the syntax with examples of 'architecture' and 'process' in VHDL.

c) Design and describe using VHDL a D-FF with negative edge triggered clock.

d) What is asynchronous input? What are techniques to interface asynchronous inputs?

Q2) Attempt any TWO **[2×8=16]**

a) Write a VHDL description to implement a 4-bit comparator. If 'A' and 'B' are 4-bit numbers; comparator has three outputs A>B, A<B and A=B.

b) Write a VHDL description for '8-bit odd parity checker'.

c) What is sequential statement? Explain syntax for 'PROCESS' statement with and without sensitivity list.

P.T.O.

Q3) Attempt any TWO **[2×8=16]**

a) Write a VHDL description for 4 bit binary up counter with 4-bit parallel load input.

b) Explain with example syntax for sub type and enumerated data type in VHDL.

c) Write a VHDL description for 8-bit priority decoder.

SECTION-II

Q4) Attempt any THREE **[3×6=18]**

a) Explain 'signal' and 'signal value' attributes with example.

b) Explain the steps for datapath designing.

c) What is LUT explain its application in FPGA.

d) What is path sensitizing in testing?

Q5) Attempt any TWO **[2×8=16]**

a) Write VHDL Code to generate 4 signals with time period 20ns; 40 ns; 80 ns; 160 ns using WAIT statements inside process.

b) Write an algorithm for counting odd numbers 1 to 19. Design data path to implement this algorithm. Derive control words for the same.

c) Design a data path for A=A+B, A= A–B, A = A AND B, A = NOT A, A = AXOR B.

Q6) Attempt any TWO. **[2×8=16]**

a) Draw and explain features XC95xx CPLD.

b) With neat diagram explain BIST testing technique.

c) With neat labeled diagram explain IOB of XC2S30 FPGA.

SF - 193

Total No. of Pages : 3

Seat No.	

T.E. (Electronics) (Part - III) (Semester - VI)
Examination, November - 2017
ELECTRONIC SYSTEM DESIGN
Sub. Code: 66855

Day and Date : Tuesday, 07 - 11 - 2017 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions :
1) **Draw neat circuit diagram wherever necessary.**
2) **Clearly specify assumptions if any.**
3) **Numbers to right indicate full marks.**
4) **Write answers to bits in questions at one place and in sequence. Do not place answers randomly.**

SECTION - I

Q1) Answer any three of the following: **[18]**

a) How various electronic systems are classified and what are different considerations for design of an electronic system?

b) Explain with neat circuit diagram, interface of TTL output with a CMOS input of ICs. Specify the input and output logic voltage levels for TTL and CMOS.

c) Explain the role of instrumentation amplifier and its importance in signal conditioning circuits for small signal sensors. (e.g. thermocouple)

d) Explain the importance of reliability considerations with the help of bath tub curve.

Q2) Answer any two of the following: **[16]**

a) When the temperature in a process is at its minimum, the sensor output is 2.48V. At maximum temperature its output is 3.9V. The ADC used to input these data into a computer has the range of 0-5V. To provide maximum resolution, design a zero and span circuit so that the signal from transducer fills the entire range of input to the ADC.

P.T.O.

b) Design a signal conditioning circuit for RTD PT-100 to get output at 10mV/°C and 0mV at 0°C, to detect temperature in the range of 0 to 50°C. Output voltage of signal conditioning circuit should be 0 to 0.5V corresponding to range of temperature in °C.

c) Design a floating I to V converter that will convert 4 to 20mA DC current signal into a 0 to 10V DC ground referenced voltage signal.

Q3) Answer any two of the following: **[16]**

a) Describe with neat timing diagram The I^2C protocol. Explain Start and Stop conditions, slave addressing and data exchange sequence.

b) Maximum analog output of DAC is required to be up to 5.12 Volts, in the step of 10 mV, what should be the reference voltage applied to DAC and what should be the bit width of DAC? And draw an interface diagram of I^2C serial DAC with any microcontroller.

c) Draw a detailed interface diagram to interface 4 no. of seven segment LED display modules to 8051 microcontroller using dynamic display interface. Use Common Anode displays modules, use Port 1 to interface segments 'a' to 'dp' and P2.0 to P2.3 lines to drive display modules. Explain the operation in short.

SECTION - II

Q4) Solve any two of following:

a) Discuss general considerations in design of ECG signal conditioner. **[9]**

b) Explain with neat circuit diagrams isolation techniques in biomedical instruments. **[9]**

c) Explain any one drug delivery system. **[9]**

Q5) Solve any one of the following: **[16]**

a) Design SMPS using LM3524 IC to provide 9 volts DC output with 500 mA current from 20V input source.

i) Draw circuit diagram for this configuration.

ii) Calculate values of resistors, inductor and capacitor for ripple voltage of 5 mV.

iii) What are criteria for selection of various components.

b) Design SMPS using LM3524 regulator to provide output voltage 12V DC with load current 100 mA. The input voltage provided is 5V DC. The ripple voltage should not exceed 30mV.

i) Draw neat circuit diagram of step-up configuration.

ii) Calculate values of resistors, inductors and capacitor.

iii) Calculate component values of oscillators for fosc = 30 KHz.

Q6) Solve any two of the following:

a) Explain the three reasons of noise coupling in the electrical and electronic circuits. **[8]**

b) Compare conducted EMI and radiated EMI. **[8]**

c) Explain the steps in PCB design and layout. **[8]**

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SF - 185

Total No. of Pages : 2

Seat No.	

T.E. (Electronics) (Part - III) (Semester - V) (Revised) Examination, November - 2017

DIGITAL COMMUNICATION

Sub. Code : 66284

Day and Date : Wednesday, 22 - 11 - 2017 **Total Marks : 100**

Time : 10.00 a.m. to 1.00 p.m.

Instructions : 1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**

SECTION - I

Q1) Answer any five: **[20]**

a) Define Random variable. Explain in brief discrete random variable and continuous random variable.

b) Explain quantization.

c) Explain scrambles and unscrambles.

d) Compare PDF & CDF.

e) Explain Auto correlation functions of Random Process.

f) What is the need of frame synchronization? Explain it.

Q2) Solve any two. **[16]**

a) For a delta modulation system

Show that the slope overload error will occur if $A > \frac{\delta fs}{2\pi fm}$.

b) Explain transmitter and receiver for the Delta modulation.

c) Explain carrier recovery circuit.

P.T.O.

Q3) Solve any two. **[14]**

a) What is the need of data formats? Explain RZ, NRZ and Manchester coding with waveforms.

b) In a PCM, using n-bits encoder. Show that signal to quantization noise ratio is given as (1.8 + 6N) dB for sine wave input.

c) Explain Gaussian Probability distribution model.

SECTION - II

Q4) Solve any two (9 marks each): **[18]**

a) With the help of neat block diagram explain the QAM transmitter and receiver.

b) Explain pseudo-noise (PN) sequence generator and List out Properties of the PN sequences with one example.

c) What is matched filter? how it can be practically realized? State its properties.

Q5) Solve any two (8 marks each):

a) Explain Coherent Binary Phase Shift Keying with required block diagram.

b) What is nyquist criterion for zero ISI? Explain it indetail.

c) With neat block diagram explain frequency hopping spread spectrum.

Q6) Solve any two (8 marks each).

a) Explain direct sequence spread spectrum. State the advantages of spread spectrum.

b) Discuss the properties and application of matched filter.

c) Explain BFSK transmitter and receiver and Draw its suitable waveform.

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SF-181

Total No. of Pages : 3

Seat No.	

T.E. (Electronics) (Semester-V) (Revised) Examination, November - 2017
SIGNALS AND SYSTEMS
Sub. Code : 66280

Day and Date : Thursday, 09-11-2017 **Total Marks : 100**

Time : 10.00 a.m. to 1.00 p.m.

Instructions : 1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume necessary data wherever required.**

SECTION-I

Q1) Attempt any two: **[16]**

a) Consider the signal x(t) as shown in Fig. 1. Sketch and label the following signals

i) $\frac{1}{2}X\left(\frac{t}{2}\right)$

ii) $X(-t-1)\,[u(t+3)-u(t+1)]$

iii) $X\left(\frac{-2t}{3}\right)$

iv) $X(3t+3)$

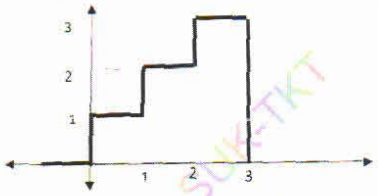

Fig. 1

b) Evaluate the convolution sum of x[n] and h[n] if
$x[n] = \delta[n] + 3\delta[n-1] + 2\delta[n-2]$ and $h[n] = \delta[n+1] + \delta[n-1]$

c) Determine even and odd part of signal $x[n]=\{2,1.5,1,\underset{\uparrow}{0}.5,0,1,2,3\}$

Q2) Attempt any two: **[16]**

a) Determine whether the following LTI system is causal and stable
i) $h[n] = 2^n\,u[-n]$

b) Determine the minimum allowable sampling frequency required to sample the signal $x(t) = 12\cos(800\pi t)\cos^2(1800\pi t)$?

c) Compute the convolution integral of the following two signal
$x(t) = u(t) - u(t-2)$
$h(t) = e^{-t}\,u(t)$

P.T.O.

Q3) Attempt any two: **[18]**

a) Explain aliasing effect? What is the use of anti-aliasing filter?

b) Determine whether the following signals are periodic or aperiodic. If the signal is periodic find the fundamental period

i) $x(t) = \cos^2(2\pi t)$

ii) $x[n] = 5 \sin(2n)$

iii) $x(t) = 2u(t) - 1/2$

c) The input-output relation for a system is given by $[n] = 2x[n] + \frac{1}{x[n-1]}$.

Is this system:

i) Static or Dynamic

ii) Causal or Non-causal

iii) Time variance or Invariance

iv) Linear or Non-Linear

SECTION-II

Q4) Attempt any two: **[18]**

a) Explain following properties of Discrete Time Fourier Transform with proof

i) Linearity

ii) Frequency Shifting

iii) Multiplication

iv) Convolution

b) Find the 4-point DFT of $x(n)$ = [2, 3, 1, 1] by direct method and verify result by matrix method.

c) Find the 4-point IDFT of X[K] = [12, –4, 0, –4] by direct method and verify result by matrix method.

Q5) Attempt any two: **[18]**

a) Find the Z-transform of the $x[n] = (2)^n u[n] + (3)^n u[-n-1]$ and sketch Region of Convergence.

b) Find Inverence Z-transform of $X[Z] = \frac{(1-e^{-a})Z}{(Z-1)(Z-e^{-a})}$ by Residue method. The sequence is right sided sequence.

c) What is Region of Convergence of Z.T.? Explain properties of Region of Convergence of Z. Transform.

Q6) Attempt any two: **[14]**

a) The transfer function of the system is $H[Z] = \frac{1+Z^{-1}}{1-0.5Z^{-1}+0.06Z^{-2}}$. Draw the direct form I and direct form II realization for the same transfer function.

b) Realize the following system in the direct form I and II

$$4\frac{d^2y(t)}{dt^2} + 2\frac{dy(t)}{dt} - 4y(t) = 2\frac{dx(t)}{dt} + 5x(t)$$

c) Realize the following system in the direct form I and II

$$y[n] + 2y[n-1] - 3y[n-2] = 2x[n] + 4x[n-1] + 3x[n-2]$$

SF-192

Total No. of Pages : 2

Seat No.	

T.E. (Electronics Engg.) (Semester-VI) Examination, November - 2017

COMPUTER ARCHITECTURE AND OPERATING SYSTEM

Sub. Code : 66854

Day and Date : Monday, 06-11-2017 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions : 1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Use suitable data if necessary.**

SECTION-I

Q1) Answer any two. **[16]**

a) Design GCD Processor. Explain with suitable example.

b) Lists various types of operating system. Explain multiprocessor Operating system in details.

c) Explain the IEEE 754 floating point number format.

Q2) Attempt any two. **[16]**

a) Design micro programmed control unit for twos compliment multiplier.

b) Perform the multiplication

i) 8*3

ii) (–5)*(4) by using Booth's algorithm

c) Explain the operating system services provided to user and to the system itself.

Q3) Attempt any three. **[3×6=18]**

a) Explain assembler, complier and linker.

b) Explain the pipeline processing with the example.

c) Write note on buffering and spooling.

d) Design hardwire control unit for DMA controller.

P.T.O.

SECTION-II

Q4) Answer any two. **[18]**

a) Explain the concept of process & threads.

b) Explain five state process Model with the help of diagram.

c) Explain the different CPU scheduling types.

Q5) Answer any two. **[16]**

a) Explain single threaded and multithreaded process models.

b) Define the terms-critical section, mutual exclusion, race condition & starvation.

c) What is monitor? Explain the structure of a monitor.

Q6) Answer any two. **[16]**

a) What is memory partitioning? Explain fixed partitioning with the help of suitable diagram.

b) Explain the concept of segmentation & paging.

c) Explain the demand paging and virtual memory concept.

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SF - 191

Total No. of Pages : 3

Seat No.	

T.E. (Electronics) (Part - III) (Semester - VI) (New) (Revised) Examination, November - 2017

POWER ELECTRONICS

Sub. Code: 66853

Day and Date : Friday, 03 - 11 - 2017 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions : 1) **All questions are compulsory.**

2) **Draw neat ckt diagram & waveforms wherever necessary.**

3) **Figures to the right indicate full marks.**

Q1) Attempt any two of the following. **[16]**

a) Draw static V. I characteristics of S.C.R. Define holding current, latching current, break over voltage. Explain the characteristics.

b) Draw and explain construction & characteristics of MOSFET.

c) Draw the dynamic characteristics of S.C.R. and give the significance of turn on and turn off time of S.C.R. in design of application circuits.

Q2) Attempt any two of the following. **[16]**

a) Explain the cosine wave firing circuit used for bridge controlled converter.

b) Explain dv/dt and di/dt protection circuits of S.C.R.

c) State differnet turn-off methods of S.C.R. and explain in detail with circuit diagram and wave form class C & class D commutation methods.

P.T.O.

Q3) Attempt any two of the following. **[18]**

a) Explain in details operation of semiconverter with waveforms for resistive load. Derive the equation of average output voltage and rms output voltage.

b) Draw the circuit diagram of mid-point converter with RL load and draw and explain the O/P waveforms.

c) A single-phase fully controlled rectifier is connected to 230 V, 50 Hz ac supply and delivering a load current of 5 Amp. The delay angle is 30°. Calculate

i) Average output voltage.

ii) Active and reactive power input.

iii) Ripple factor of the output voltage.

iv) Input power factor.

v) RMS value of the fundamental component of input current.

Q4) Attempt any two of the following. **[16]**

a) Explain the different voltage control techniques of the chopper.

b) Explain the operation of step down chopper with RL load. Also draw its output voltage, current waveform & derive the equation of O/P. voltage.

c) A step-up chopper with pulse width of 150μ.sec. is operating on 220V.Dc. supply. Compute load voltage if blocking period of device is 40μ.sec.

Q5) Attempt any two of the following. **[16]**

a) Explain in detail operation of single phase half bridge inverter with R. Load & also derive the equation of rms output voltage?

b) Explain the sine wave and modified sine wave PWM technique used for harmonic reduction in inverter?

c) Derive the equation for harmonic analysis of a square wave inverter.

Q6) Attempt any three of the following. **[18]**

a) Explain the operation of light dimmer using triac and diac circuit.

b) Explain AC voltage stabilizer using relays.

c) Draw the circuit diagram of single phase preventer and explain its operation.

d) With neat block diagram explain online and offline UPS.

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SF-183

Total No. of Pages : 3

Seat No.	14385

T.E. (Electronics) (Semester-V) Examination, November - 2017

ELECTROMAGNETIC ENGINEERING

Sub. Code : 66282

Day and Date : Tuesday, 14 - 11 - 2017 **Total Marks : 100**

Time :10.00 a.m. to 1.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicates full marks.**
3) **Assume suitable data if necessary.**
4) **Use of non-programmable calculator is allowed.**
5) **Use Smith chart if necessary.**

SECTION-I

Q1) Attempt any two. **[16]**

a) Find the expression for Electric field intensity E & Electric flux density D at a point due to line charge with uniform charge density due to charge density ρ_L c/m.

b) Derive the expression for Divergence of D.

c) A charge of –0.3 μC is located at A(25,–30,15) cm, and a second charge of 0.5 μC is located at B(–10,8,12)cm. Find E at
   i) origin;
   ii) (15,20,50)cm.

Q2) Attempt any two. **[16]**

a) Use Ampere's law to determine the magnetic field intensity H at point P due to
   i) Infinite filament,
   ii) Uniform sheet.

b) Vector magnetic potential $A=(x^2+y^2)\,a_z$ μwb/m², determine the magnetic field produced by current element at (1,2,3) in free space.

c) Current element $Idl=10^{-4}\,(4a_x - 3a_y + a_z)$ A.m, located at A (5,–2,3), produces field dH at B(4,–1, 2).
   i) Give unit vector in the direction of dH at B;
   ii) Find |dH|

P.T.O.

Q3) Attempt any three. **[18]**

a) Explain Biot-Savart Law.

b) Derive the expression for Energy density in static electric field.

c) Given points A (8,–5,4) & B(–2,3,2), find

i) the distance form A to B,

ii) a unit vector directed from A to B,

iii) unit vector directed from origin towards midpoint of line AB.

d) Transform the given vector to spherical co-ordinates at the points given

i) 10 a_x at point P(–3, 2, 4);

ii) 10 a_y at point Q(5, 30°, 4)

SECTION-II

Q4) Solve any Two. **[16]**

a) Give the comparison between circuit theory and field theory.

b) A lossless transmission line is 80cm long and operates at a frequency of 600 MHz. The line parameters are L = 0.25 μH/m and C = 100 pf/m. Find the characteristic impedance, the phase constant and phase velocity.

c) A plane electromagnetic wave travelling in the + ve z direction is an unbounded lossless dielectric medium with μ_r=1, ε_r = 3 has peak electric field intensity E of 16 v/m. find v, η, magnitude of H and peak value of Poynting vector.

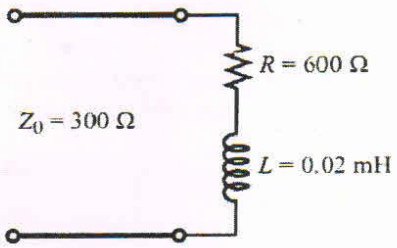
Q5) Solve any Two. **[16]**

a) What is characteristic impedance? Derive transmission line equations.

b) A 300-Ω lossless air transmission line is connected to a complex load composed of a resistor in series with an inductor, as shown in Fig. At 5 MHz, determine:

i) Reflection coefficient Γ,

ii) SWR



c) Find the amplitude of the displacement current density in air, where local FM station provides a carrier having H = 0.4 cos [2.10 $(3\times10^8 t - x)$] a_z A/m.

Q6) Solve any Three. **[18]**

a) Faraday's law

b) Circuit applications of the Poynting vector.

c) Group and phase velocity.

d) Smith chart.

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SF-189

Total No. of Pages : 2

Seat No.	

T.E. (Electronics) (Semester - VI) (Revised) (New) Examination, November - 2017
DIGITAL SIGNAL PROCESSING
Sub. Code : 66851

Day and Date : Wednesday, 01 - 11 - 2017 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions : 1) **Figures to the right indicate full marks.**
2) **Assume suitable data if required.**

SECTION - I

Q1) Attempt any two : **[18]**

a) Explain in detail Radix 2, DIT FFT Algorithm.

b) Explain in detail Overlap Save method of Sectioned Convolution.

c) Explain in detail any four properties of DFT.

Q2) Attempt any two : **[16]**

a) Explain in detail relationship between DFT and Z Transform.

b) Explain any four applications of Wavelet Transform.

c) What are the advantages and disadvantages of FIR Filters? What is the necessary and sufficient condition for the linear phase characteristic of an FIR Filter?

Q3) Attempt any two : **[16]**

a) Design a FIR high pass filter with cutoff frequency of 1.5 KHz and sampling frequency of 5 KHz with 7 samples using Fourier Series Method. Determine the frequency response.

b) Compare any four types of window functions used in Design of FIR Filters.

c) Explain in detail design of FIR filter using Kaiser Window.

P.T.O.

SECTION - II

Q4) Attempt any two : **[18]**

a) Compare the Impulse invariant Transformation and Bilinear Transformation Method.

b) Explain in steps how to Design Low pass Butterworth Digital IIR filter.

c) Design a Chebyshev digital IIR low pass filter using bilinear transformation by taking T = 1 second, to satisfy the following specifications

$0.8 \leq |H(e^{j\omega})| \leq 1.0$; for $0 \leq \omega \leq 0.2\pi$

$|H(e^{j\omega})| \leq 0.2$; for $0.32\pi \leq \omega \leq \pi$ or

By taking pass band ripple $\leq$ 1.9 dB,

Stop band attenuation $\geq$ 13.97 dB,

Pass band edge frequency = 0.2π rad/sample

Stop band edge frequency = 0.32π rad/sample

Q5) Attempt any two : **[16]**

a) Explain in detail general Architecture of TMS320C67XX.

b) What is meant by finite word length effects in digital filters? List and explain.

c) Draw the direct form structure of the FIR systems described by the following equation

$$y(n)=x(n)+\frac{1}{2}x(n-1)+\frac{1}{4}x(n-2)+\frac{1}{6}x(n-3)+\frac{1}{8}x(n-4)$$

Q6) Attempt any two : **[16]**

a) What are the applications of Multi-rate digital filter?

b) Define Upsampling and Downsampling. Explain two stage Interpolator.

c) Explain in detail sampling rate conversion by rational factor $\frac{I}{D}$.